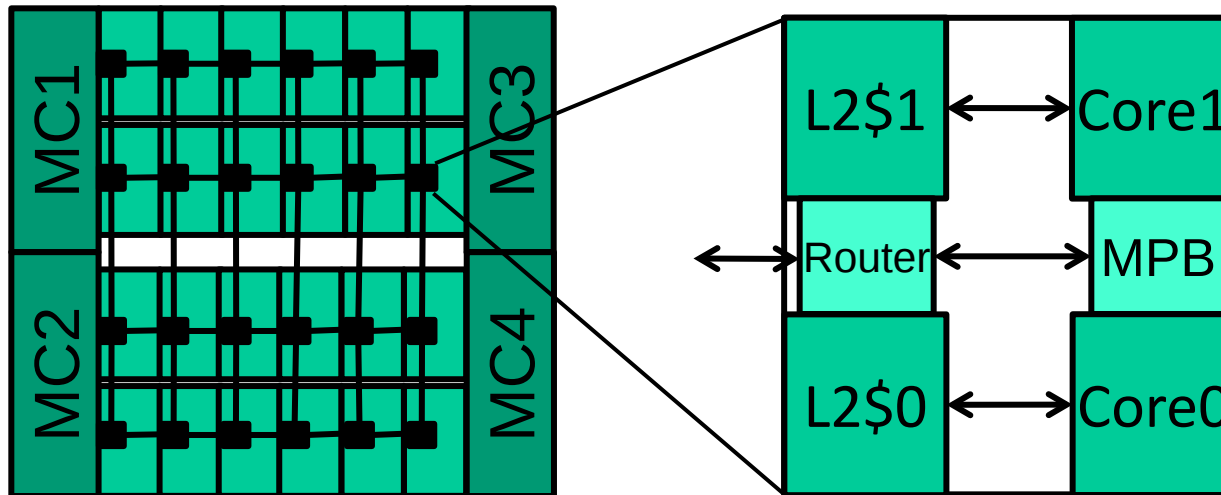


Performance Tuning of SCC-MPICH by means of the Proposed MPI-3.0 Tool Interface

- The Intel *Single-Chip Cloud Computer* (SCC)
→ an 48-cores Research Processor by Intel
- SCC-MPICH
→ yet another MPI Library for the Intel SCC
- The Proposed MPI-3.0 Tool Interface
→ for querying MPI library *internal* information

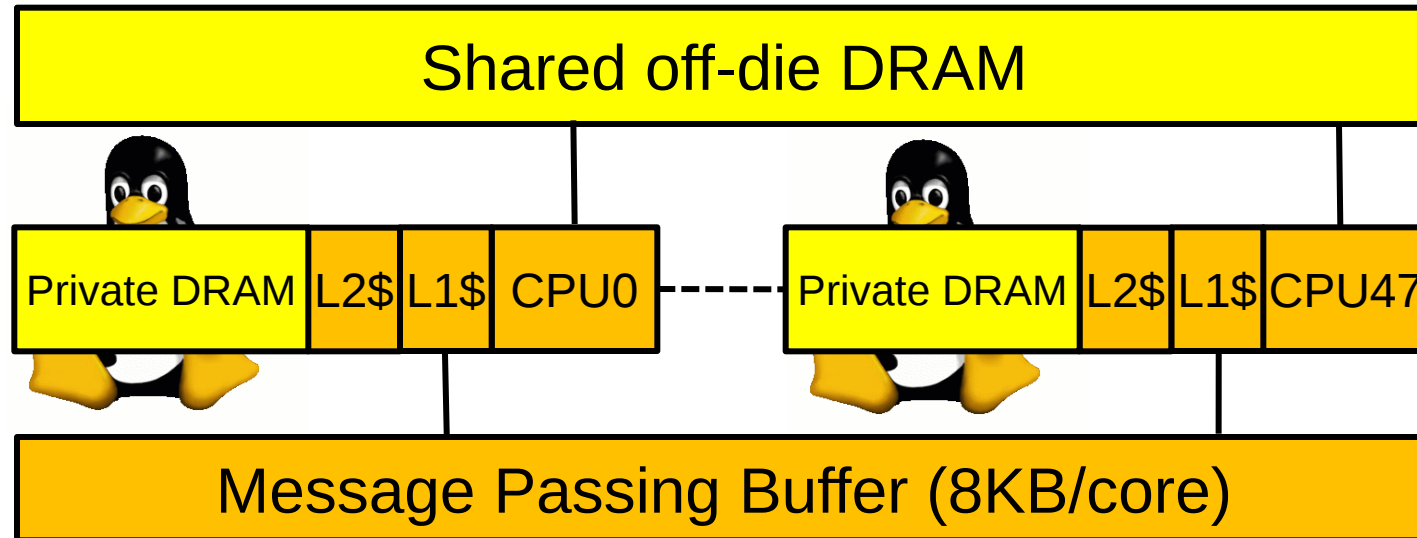
The Intel SCC Many-core Processor

- Intel Single-Chip Cloud Computer
→ a *Concept Vehicle* for Many-core Software Research
- 48 Pentium-I Cores arranged in a 6x4 on-die Mesh
→ 2 Cores and 1 Router per *Tile*

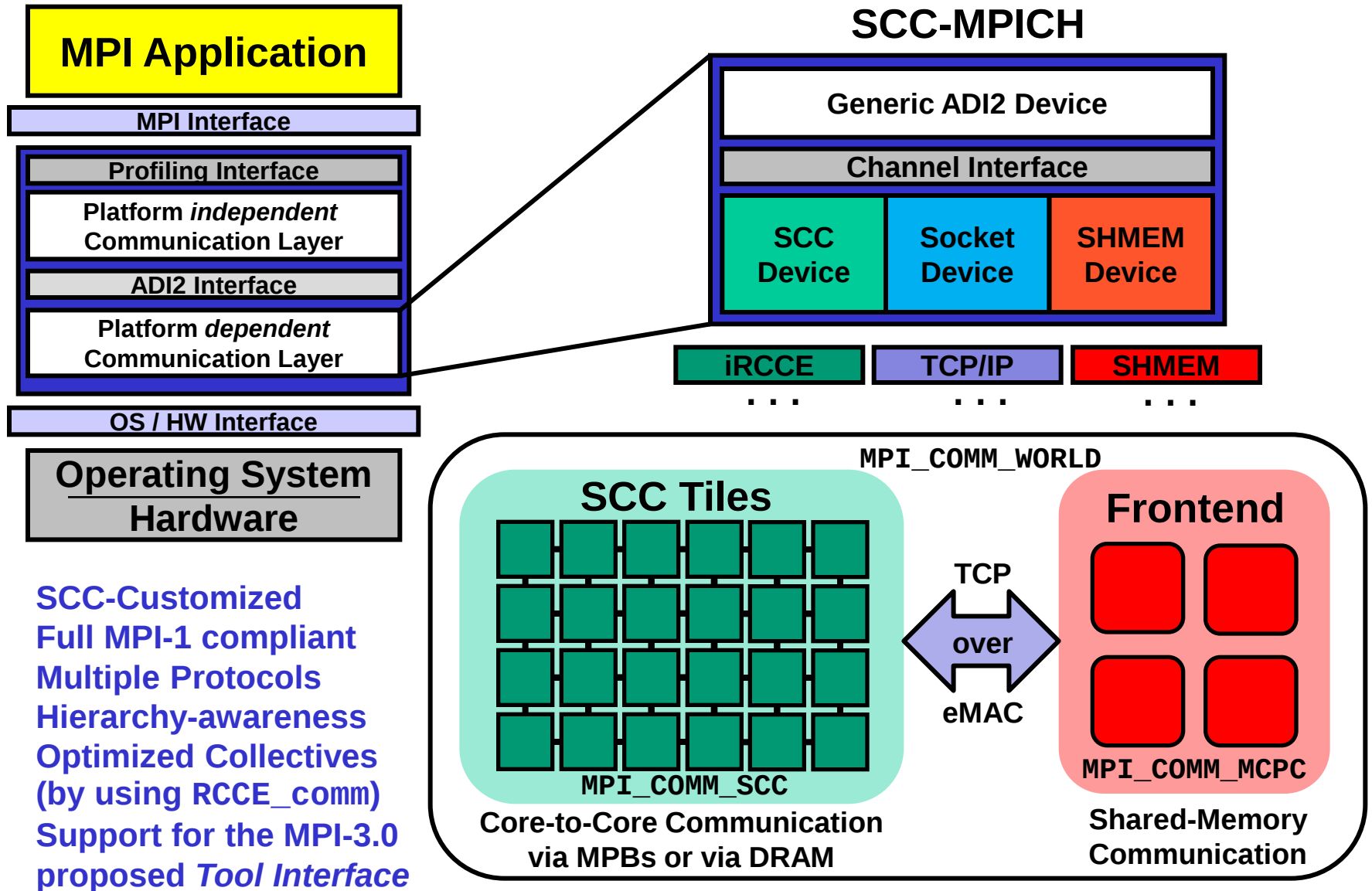


- On-die *Message-Passing Buffers* (MBP) / 16kByte per Tile
→ accessible as distributed on-die *Shared-Memory*
- 4 on-die Memory Controllers (MC1-4)
→ max. 64GByte DDR3 off-die main memory

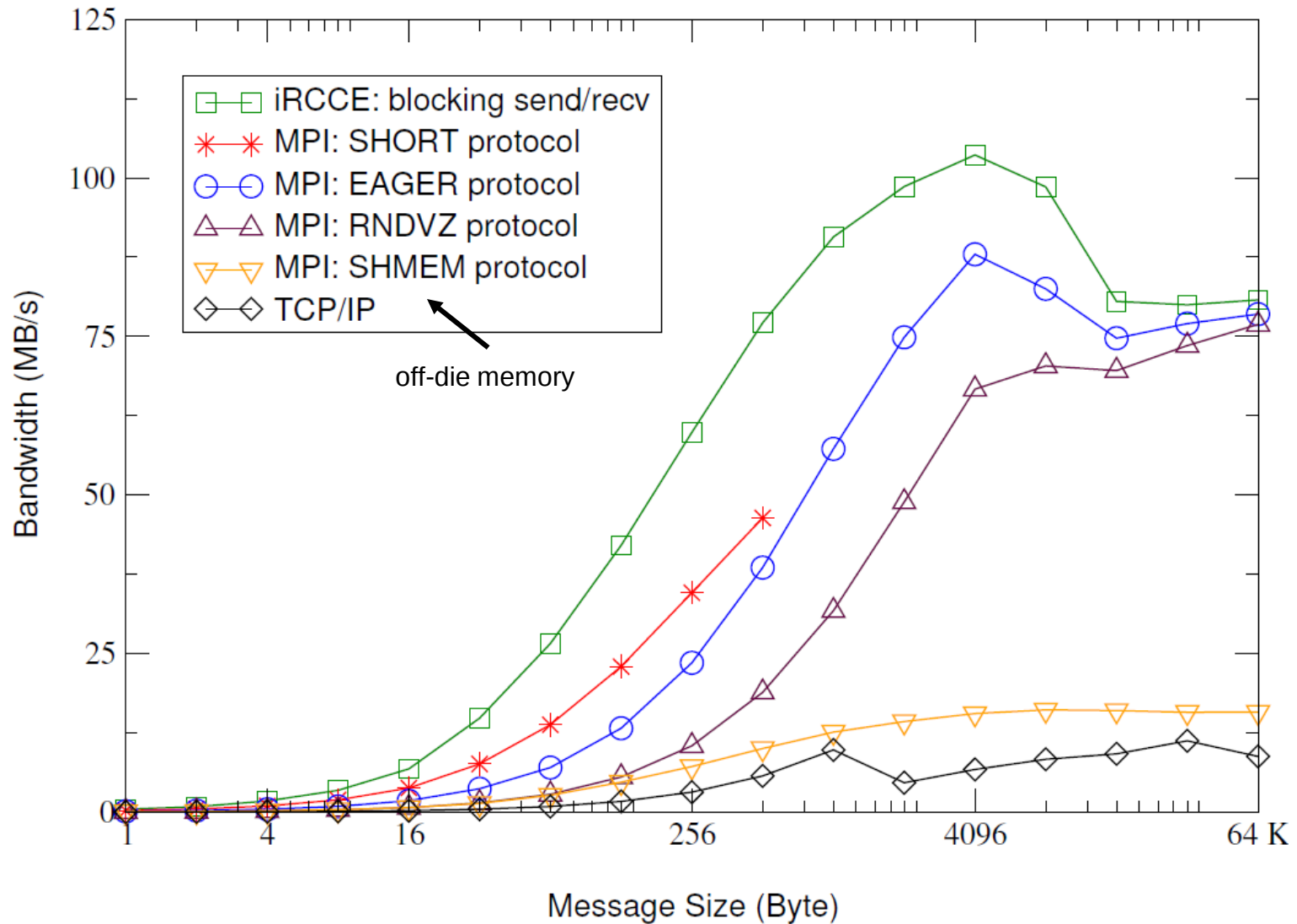
- **Strictly No Cache Coherency**
→ Cluster-on-Chip Architecture
- **Private off-die DRAM Regions (one per Core)**
→ *Caches enabled!* One *Linux* instance per Core!



- **Shared / Global off-die DRAM Region**
→ *Caches disabled* per default! → e.g. for global shared data
- **Shared on-die MPB Regions**
→ Cached in L1, L2 Bypass / Fast L1 Invalidation for MPB-Data



Ping-Pong Measurements



Tile: 533MHz, Mesh: 800MHz, DDR: 800MHz

- The MPI Tool Interface:

<code>MPI_T_Cvar_get_info()</code>	}	<i>for Control Variables</i>
<code>MPI_T_Cvar_read()</code>		
<code>MPI_T_Cvar_write()</code>		
...		

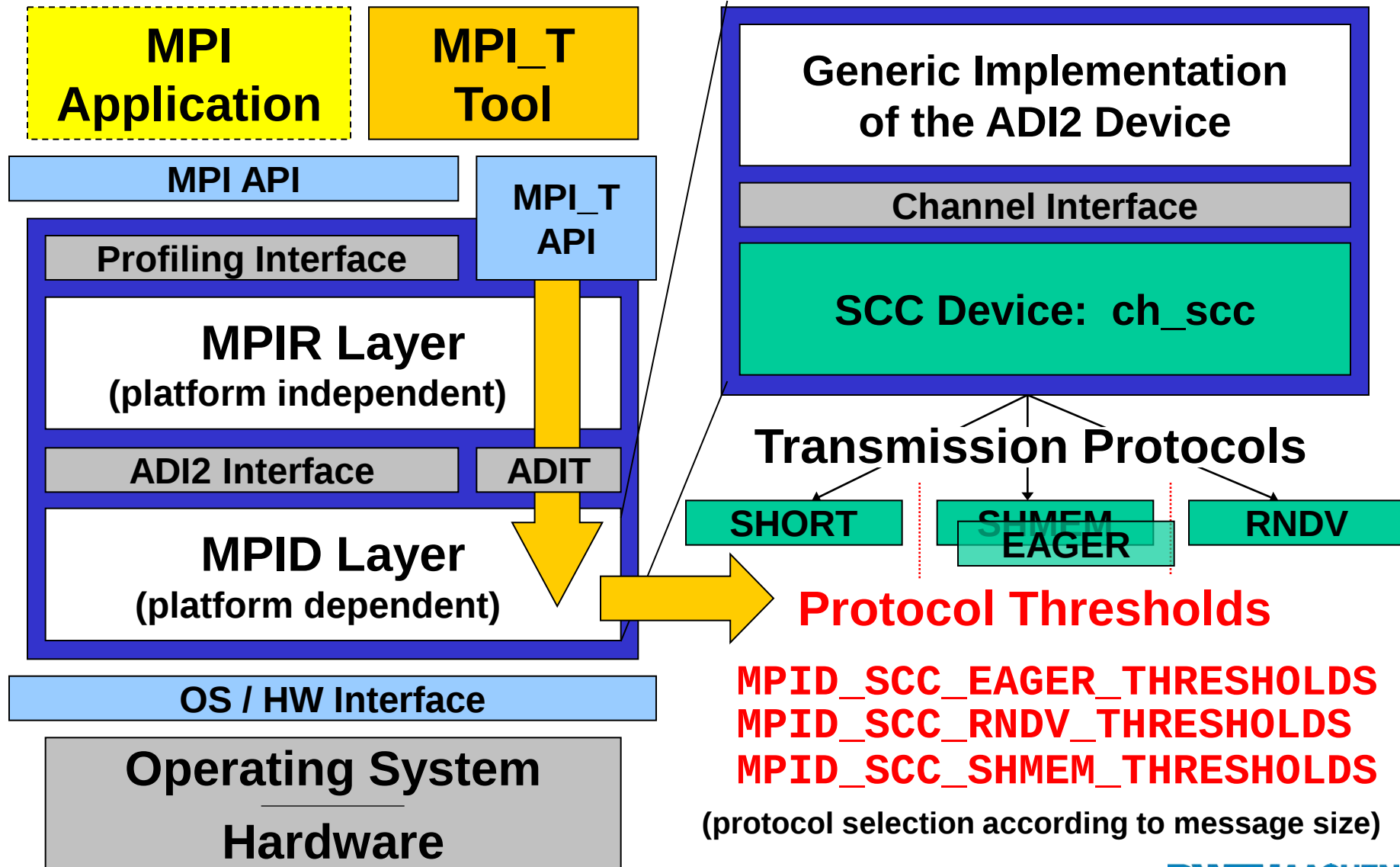
- Prototyping the MPI Tool Interface in SCC-MPICH:

<code>MPID_SCC_RNDV_THRESHOLDS</code>	}	<i>Control Variables</i>
<code>MPID_SCC_EAGER_THRESHOLDS</code>		
<code>MPID_SCC_SHMEM_THRESHOLDS</code>		
...		

<code>MPID_SCC_MSGS_SENT</code>	}	<i>Performance Counters</i>
<code>MPID_SCC_MSGS_RECEIVED</code>		
<code>MPID_SCC_MSGS_UNEXPECTED</code>		
...		

The Proposed MPI-3.0 Tool Interface

MPI_T_Cvar_write()



Thank you for your attention!

Carsten Clauss
Chair for Operating Systems
RWTH Aachen University
clauss@lfbs.rwth-aachen.de

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